**Digital Circuits and Systems** 

End Semester Exam

Date: 26th Nov. 2012 Time: 180 Minutes Max Marks. 80

Notes: All questions are compulsory.

Marks of each question are mention against it.

Assumptions made should be written clearly.

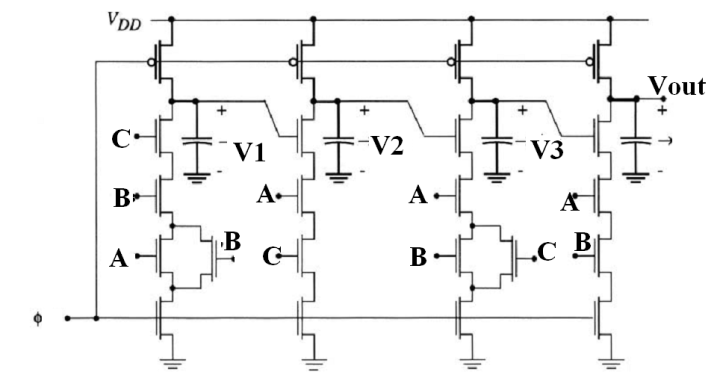
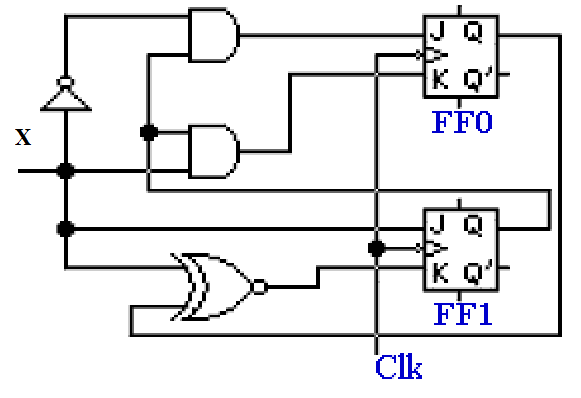
**1:** Using a module-16 binary counter with parallel inputs, implement a counter that counts the following periodic sequence: 1,2,7,8,9.  **[10]**

**2:** Design a sequential network which repeatedly generates the sequence “10011”**. [10]**

**3:** Design a sequential circuit using serial in parallel out register that recognizes the sequences 01011 and 10111. **[5]**

**4:** Using 3 number of modulo 16 counters implement 18 to 314 counter with cascade as well as parallel implementation. (Note that 314 is last state that the counter have to produce) **[3 + 7]**

**5:** Analyze the circuit given in figure 1 and draw the corresponding state diagram **[7]**

**6:** Analyze the circuit shown in figure 2 and write the minimized expressions for V1, V2, V3 and Vout. **[8]** 

**Figure 1 figure 2**

**7:** Design a sequential system whose state transition table is shown below. **[10]**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Present State** | **Next state for Input =** | | | | **Output** |
|  | **0** | **1** | **2** | **3** |  |
| 000 | 000 | 001 | 000 | 111 | 000 |
| 001 | 001 | 011 | 000 | 111 | 001 |
| 010 | 010 | 101 | 001 | 111 | 010 |
| 011 | 011 | 111 | 001 | 111 | 011 |
| 100 | 100 | 001 | 010 | 111 | 100 |
| 101 | 101 | 011 | 010 | 111 | 101 |
| 110 | 110 | 101 | 011 | 111 | 110 |
| 111 | 111 | 111 | 011 | 111 | 111 |

**8:**

1. Implement a rising edge triggered D flip flop using multiplexers. **[3]**
2. Implement a Dual edge triggered D flip flop. Dual edge triggered flip flop means it can operate at both rising as well as falling edge of the clock. (Hint Use multiple D single edge triggred flip flops with MUXes) **[7]**

**9:** Design sequential circuit that produces the output waveform with time period equal to 5 times of the input waveform and duty cycle of the output waveform is 60% i.e. It is high for initial 60% of the time and low for remaining 40% time duration. (Hint you can use some counter with focus on a separate output variable which would produce output waveform). **[10]**

**Bonus Questions:**

**(Please attempt these questions in the end. Final weightage of exam would be out of 80 only, this is just a bonus to make-up for marks lost in other exams or quizzes).**

**1:** A snail leaves his warm house and takes a crawl through the forest leaving behind him on the ground a trail of “0″s and “1″s. He takes a very complicated route crossing his path several times. At one point he becomes tired and disoriented and wishes to go back home. He sees his own path of “0″s and “1″s on the ground which he is about to cross (i.e. not the trail ending in his tail) and wonders whether to follow the trail towards the left or towards the right.  
What is the shortest repeating code of “0″s and “1″s he should leave as he crawls in order to easily and deterministically track the way back home? What is the minimum amount of bits he needs to observe (or the sample length of the code)?

**(Please be very logical in your answer, any illogical story won’t give you partial marks)**  **[20]**

**2:** Consider a binary number system with base **-2** (minus two). This number system is more commonly known as negabinary number system. Try writing the decimal equivalents of 0-9 in this system. If you are able to do so, then give a method to add two negabinary numbers. **[10]**